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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/687,493
Filing Date	10/13/2000
First Named Inventor	Sung Sik Jang
Art Unit	2826
Examiner Name	Williams, Alexander O.
Attorney Docket Number	AMKOR-045A

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- [X] Fee Transmittal Form
- [X] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [X] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)_____
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Other Enclosure(s) (please Identify below): Certificate of Mailing; and Return Receipt Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Mark B. Garred STETINA BRUNDA GARRED & BRUCKER - Customer No. 007663
Signature	
Date	8/10/04

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Signature	Andrea K Levine	Date	08/10/2004

PTO/SB/17 (10-03)
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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 130.00

Complete if Known	
Application Number	09/687,493
Filing Date	10/13/2000
First Named Inventor	Sung Sik Jang
Examiner Name	Williams, Alexander O.
Art Unit	2826
Attorney Docket No.	AMKOR-045A

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

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Deposit Account Number: 19-4330

Deposit Account Name: Stetina Brunda Garred & Brucker

The Director is authorized to: *(check all that apply)*

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X	=	
Independent Claims		- 3** =		X	=	
Multiple Dependent					=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	130.00
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 130.00

SUBMITTED BY

(Complete *(if applicable)*)

Name *(Print/Type)*	Mark B. Garred	Registration No. *(Attorney/Agent)*	34,823	Telephone	949-851-1246
Signature				Date	3/10/04

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ATTORNEY DOCKET NO: AMKOR-045A
TITLE: SEMICONDUCTOR PACKAGE HAVING IMPROVED ADHESIVENESS AND GROUND BONDING

Certificate of Mailing under 37 CFR 1.8 or 37 CFR 1.10

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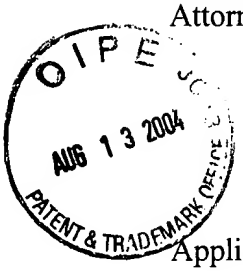
7. A Check for $130.00; and
8. Return Receipt Postcard

Application No.: 09/687,493
Attorney Docket: AMKOR-045A



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Sung Sik Jang	Confirmation No.	9392
Serial No.:	09/687,493	Art Unit:	2826
Filed:	10/13/2000	Examiner:	Williams, Alexander O.
For:	Semiconductor Package Having Improved Adhesiveness and Ground Bonding		

PETITION TO ACCEPT SUBMISSION OF RESPONSE AFTER ALLOWANCE UNDER 37 C.F.R. §1.312

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

Applicant hereby submits this Petition in accordance with provisions of 37 C.F.R. Section 1.312.

A Notice of Allowance was issued in relation to the present application on April 14, 2004. On June 18, 2004, the Issue Fee and Formal Drawings were filed in relation to the present application. This Petition is accompanied by the required fee of $130.00

This submission is in direct response to a specific request by Examiner Williams in a telephonic communication with Applicant's counsel on August 5, 2004. More particularly, Examiner Williams indicated that as a result of an internal review procedure at the U.S. Patent and Trademark Office, Applicant was requested to submit a complete "clean" copy of the specification of the present application in its current, amended form. In response to this request, attached hereto as Exhibit A is the requested clean copy of the specification. Attached hereto as Exhibit B is a marked-up version of the specification reflecting the various changes that have been made thereto during the prosecution of the present application.

08/13/2004 SDIRETAE 00000026 09687493
01 FC:1460 130.00 OP

If any additional fee is required, please charge Deposit Account Number 19-4330.

Respectfully submitted,

Date: 8/10/04 By: _____

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Case No.: AMKOR-045A

EXHIBIT A

CLEAN SPECIFICATION

SEMICONDUCTOR PACKAGE HAVING IMPROVED ADHESIVENESS AND GROUND BONDING

SUNG SIK JANG

BACKGROUND OF THE INVENTION

TECHNICAL FIELD OF THE INVENTION

[0001] The various embodiments of the present invention relates in general to a semiconductor package and, more particularly but not by way of limitation, to a semiconductor package in which the adhesiveness between a chip paddle and a package body is improved, and the chip paddle ground-bonding is improved.

HISTORY OF RELATED ART

[0002] It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method of and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal leadframes for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the leadframe are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this

design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

[0003] As set forth above, the semiconductor package therein described incorporates a leadframe as the central supporting structure of such a package. A portion of the leadframe completely surrounded by the plastic encapsulant is internal to the package. Portions of the leadframe extend internally from the package and are then used to connect the package externally. More information relative to leadframe technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski and incorporated by reference herein. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York.

[0004] Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically includes a motherboard on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. Not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

[0005] According to such miniaturization tendencies, semiconductor packages, which transmit electrical signals from semiconductor chips to motherboards and support the semiconductor chips on the motherboards, have been designed to have a small size. By way of example only, such semiconductor packages may have a size on the order of 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

[0006] However, this conventional semiconductor package is problematic in that a thickness of the silver plated layer formed on the upper faces of the chip paddle and the internal leads deteriorates the adhesiveness between the package body and the chip paddle or the internal leads. That is, the silver-plated layer is very weakly bonded to the

package body of the encapsulation material (the chip paddle or the side of the internal lead, both of which are made of copper, are strongly bonded to the package body), so that interfacial exfoliation is easily caused at the boundary between the package body and the silver-plated layer. Further, moisture can readily permeate the semiconductor package through the exfoliated portion, which may cause the semiconductor package to crack.

[0007] Usually a semiconductor chip or a chip paddle is ground-bonded by conductive wires to achieve grounding or eliminate electrical noise problems. In this conventional semiconductor package, the semiconductor chip is similar in area to the chip paddle, so that there are no sufficient areas for ground bonding.

BRIEF SUMMARY OF THE INVENTION

[0008] In one embodiment of the present invention, there is provided a semiconductor chip having an upper surface and a bottom surface. A plurality of input bond pads and output bond pads on the upper surface of the semiconductor chip and along the perimeter of the semiconductor chip are electrically connected to the semiconductor chip. A chip paddle is provided which has a top surface, a side surface and a bottom surface. The chip paddle is bonded to the bottom surface of the semiconductor chip by an adhesive. The chip paddle has corners, a perimeter and a half-etched section at the lower edge of the chip paddle along the chip paddle perimeter.

[0009] A leadframe is provided having a plurality of tie bars. Each of the tie bars has a side surface and a bottom surface. Each of the tie bars is connected to the corners of the chip paddle and externally extends from the chip paddle and has a half-etched section. A plurality of dam bars is provided on the leadframe to help limit flow of encapsulation material on the leadframe.

[0010] A plurality of internal leads connects to the leadframe. Each of the leads has a side surface and a bottom surface. The leads are radially formed at regular intervals along and spaced apart from the perimeter to the chip paddle and extend towards the chip paddle. Each of the leads has a step shaped half-etched section facing the chip paddle.

[0011] A ground ring is provided having an upper surface and a lower surface, and positioned between the semiconductor chip and the plurality of internal leads. The

ground ring may interchangeably be used as a ground or a power ring. The upper surface of the ground ring is substantially planar with the upper surface of the semiconductor chip and the upper surface of the plurality of internal leads. A plurality of conductive wires is electrically connected to the plurality of internal leads and the semiconductor chip, wherein the conductive wires have a loop height between the leads and the semiconductor chip. Because of the planarity of the grounding leads and semiconductor chip, the loop height of the conductive wires is minimized, which allows smaller packaging.

[0012] Encapsulating material encapsulates the semiconductor chip, conductive wires, chip paddle, and the leads to form a package body. The flow of the encapsulation material is limited by the dam bars formed on the leadframe. After encapsulation, the chip paddle, leads, and tie bars are externally exposed at respective side and bottom surfaces. The chip paddle further has through-holes in the half-etched section of the chip paddle for increasing the bonding strength of the encapsulation material in the package body. In addition, tabs in the half-etched section of the chip paddle may be provided for the same purpose.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] A more complete understanding of the method and apparatus of the present invention may be obtained by reference to the following detailed description with like reference numerals referring to like elements when taken in conjunction with the accompanying Drawings wherein:

[0014] FIGURE 1 is a top plan view of one embodiment of the semiconductor package of the present invention;

[0015] FIGURE 2 is a side elevation cross-section view of the semiconductor package of FIGURE 1 taken along line 2-2;

[0016] FIGURE 3 is a side elevation cross-section view of the semiconductor package of FIGURE 1 taken along line 3-3;

[0017] FIGURE 4 is a top plan view of an alternate embodiment for the semiconductor package of the present invention; and

[0018] FIGURE 5 is a side elevation cross-section view of the semiconductor package of FIGURE 4 taken along line 6-6.

DETAILED DESCRIPTION OF THE INVENTION

[0019] Referring first to FIGS. 1 through 3, a semiconductor package 10 is shown construed in accordance with the principals of the present invention. The semiconductor package 10 includes a semiconductor chip 20 having an upper surface 30, a perimeter 40 and a bottom surface 50. A plurality of input bond pads 60 and output bond pads 70 is disposed on the upper surface 30 of the semiconductor chip 20. A chip paddle 80 having a top surface 90, a side surface 100 and a bottom surface 110 is secured to the bottom surface 50 of the semiconductor chip 20 via an adhesive 120. The chip paddle 80 has corners 130, a perimeter 140 and a half-etched section 150. The half-etched section 150 is located at a lower edge 160 of the chip paddle 80.

[0020] Referring now to FIGS. 1 through 3 in combination, a leadframe 170 is shown having a plurality of tie bars 180, a side surface 190 and a bottom surface (not shown). The tie bars 180 are connected to the corners 130 of the chip paddle 80. The tie bars 180 externally extend from the chip paddle 80. The leadframe 170 further has a plurality of dam bars 220.

[0021] A plurality of leads 230 are connected to the leadframe 170 and have an upper surface 235 and a bottom surface 250. The leads 230 are radially formed at regular intervals along the perimeter 140 and spaced apart from the perimeter 140 of the chip paddle 80. The leads 230 extend towards the chip paddle 80, such that each of the plurality of leads 230 has a half-etched section 260 facing the chip paddle 80. It is to be noted that the hatched areas in FIG. 1 are the half-etched sections of the paddle 80 and leads 230.

[0022] Referring to FIG. 2, there is disclosed a ground ring 262 formed in the half-etched section 150 of the chip paddle 80. The ground ring 262 is positioned between the semiconductor chip 20 and the plurality of leads 230. The ground ring 262 may be interchangeably used as a power ring should circumstances require. The upper surface

264 of the ground ring 262 is planar with the upper surface 90 of the chip paddle 80 and the upper surface 235 of the leads 230.

[0023] A plurality of conductor wires 270 is provided and electrically connected to the plurality of leads 230 and the semiconductor chip 20. The plurality of conductive wires 270 have a loop height 275 between the plurality of leads 230 and the semiconductor chip 20. The loop height 275 of the conductive wires 270 is minimized from the upper surface 235 of the leads 230 and the upper surface 30 of the semiconductor chip 20.

[0024] To form the semiconductor package 10, encapsulation material 280 encapsulates the semiconductor chip 20, conductive wires 270, chip paddle 80, and leads 230. The dam bars 220 limit the flow of the encapsulation material 280 on the leadframe 170. During encapsulation, the chip paddle 80, leads 230, and tie bars 180 are externally exposed at the respective side and bottom surfaces. In one embodiment, the chip paddle 80 is provided with a plurality of through holes 300 in the half-etched section 150 for increasing the bonding strength of the encapsulation material 280 with the package 10.

[0025] The through holes 300 (Fig. 1) may be formed by chemical etching, such as when patterning the entire leadframe 170 for forming the half-etched section 150 of the chip paddle 80. Alternatively, the through holes 300 (Fig. 1) may be formed by the use of a mechanical punch or similar device. It should be noted that other methods may be used to form the through holes 300, and the various embodiments of the present invention are not limited by the formation techniques disclosed herein.

[0026] Referring now to Fig. 4 and FIG. 5, an alternate embodiment for a semiconductor package 11 is shown. In this embodiment, the chip paddle 80 is provided with a plurality of tabs 310 in the half-etched section 150 of the chip paddle 80 for the similar purpose of increased bonding strength. It is also contemplated that the combination of through holes 300 (Fig. 1) and tabs 310 may be used to increase the bonding strength of the encapsulation material 280 in the package 10.

[0027] The tabs 310 are formed in the half-etched section 150 of the chip paddle 80. The tabs 310 must extend to a limited degree to prevent a short circuit forming between the tabs 310 and the leads 230. It is preferable that the number of the tabs 310 corresponds to the number of the grounding input bond pads 60 and output bond pads 70

of the semiconductor chip 20. The tabs 310 may be formed by chemical etching when patterning the entire leadframe 171 and also by other mechanical methods depending on the requirements of the individual package 11. By increasing the area or length of the chip paddle 80, the tabs 310 are easily bonded with conductive wires 270 by increasing the area for which to connect the conductive wires 270. The tabs 310 may serve to function as a ground or power ring in certain applications. It is to be noted that the hatched areas in FIG. 4 are the half-etched sections of the paddle 80 and leads 230.

[0028] The tab 310 is electrically connected to the semiconductor chip 20 via conductive wire 270.

[0029] As described previously, the use of the through holes 300 and tabs 310 increases the bonding strength to the encapsulation material 280, in addition to improving the fluidity of the encapsulation material 280 upon encapsulating. The presence of the through holes 300 and tabs 310 improves the fluidity of encapsulation material 280 by directing flow over or through the tabs 310 and through holes 300 in the package 10. In certain embodiments, as shown in FIGS. 2 and 3, a plated layer 320 may be applied to the upper surfaces 90, 235 of the chip paddle 80 and leads 230, respectively, to increase bonding strength to the wires 270.

[0030] It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. While the semiconductor package having improved adhesiveness and crown bonding shown as described is preferred, it will be obvious to a person of ordinary skill in the art that various changes and modifications may be made therein without departing from the spirt and scope of the invention.

[0031] The previous description is of a preferred embodiment for implementing the invention, and the scope of the invention should not necessarily be limited by this description. The scope of the present invention is instead defined by the following claims.

[0032] The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein:

U.S. Patent No.	Title of Application	First Named Inventor
6,501,161	Semiconductor Package Having Increased Solder Joint Strength	Kil Chin Lee
6,667,662	Clamp and Heat Block Assembly for Wire Bonding a Semiconductor Package Assembly	Young Suk Chung
6,639,308	Near Chip Size Semiconductor Package	Sean Timothy Crowley
6,753,597	Semiconductor Package	Sean Timothy Crowley
6,605,866	Stackable Semiconductor Package and Method for Manufacturing Same	Sean Timothy Crowley
6,730,544	Stackable Semiconductor Package and Method for Manufacturing Same	Jun Young Yang
6,616,436	Method of and Apparatus for Manufacturing Semiconductor Packages	Hyung Ju Lee
6,555,899	Semiconductor Package Leadframe Assembly and Method of Manufacture	Young Suk Chung

[0033] It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments.

It will be obvious to a person of ordinary skill in the art that various changes and modifications may be made herein without departing from the spirit and scope of the invention.

Case No.: AMKOR-045A

EXHIBIT B

MARKED-UP SPECIFICATION

SEMICONDUCTOR PACKAGE HAVING IMPROVED ADHESIVENESS AND GROUND BONDING

~~TECHNICAL FIELD~~ **SUNG SIK JANG**

BACKGROUND OF THE INVENTION

TECHNICAL FIELD OF THE INVENTION

[0001] The **various embodiments of the** present invention relates in general to a semiconductor package~~,~~ and**,** more particularly but not by way of limitation, to a semiconductor package in which the adhesiveness between a chip paddle and a package body is improved, and the chip paddle ground-bonding is improved.

HISTORY OF RELATED ART

[0002] It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method of and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal leadframes for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the leadframe are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this

design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

[0003] As set forth above, the semiconductor package therein described incorporates a leadframe as the central supporting structure of such a package. A portion of the leadframe completely surrounded by the plastic encapsulant is internal to the package. Portions of the leadframe extend internally from the package and are then used to connect the package externally. More information relative to leadframe technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski and incorporated by reference herein. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York.

[0004] Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically includes a motherboard on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. ~~These electronic appliances are typically manufactured in reduced sizes and at reduced costs, consumer demand increases. Accordingly, not~~ **Not** only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

[0005] According to such miniaturization tendencies, semiconductor packages, which transmit electrical signals from semiconductor chips to motherboards and support the semiconductor chips on the motherboards, have been designed to have a small size. By way of example only, such semiconductor packages may have a size on the order of 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

[0006] However, this conventional semiconductor package is problematic in that a thickness of the silver plated layer formed on the upper faces of the chip paddle and the internal leads deteriorate**s** the adhesiveness between the package body and the chip

paddle or the internal leads. That is, the silver-plated layer is very weakly bonded to the package body of the encapsulation material (the chip paddle or the side of the internal lead, both of which are made of copper, are strongly bonded to the package body), so that interfacial exfoliation is easily caused at the boundary between the package body and the silver-plated layer. Further, moisture can readily permeate the semiconductor package through the exfoliated portion, which may cause the semiconductor package to crack.

[0007] Usually a semiconductor chip or a chip paddle is ground-bonded by conductive wires to achieve grounding or eliminate electrical noise problems. In this conventional semiconductor package, the semiconductor chip is similar in area to the chip paddle, so that there are no sufficient areas for ground bonding.

BRIEF SUMMARY OF THE INVENTION

[0008] In one embodiment of the present invention, there is provided a semiconductor chip having an upper surface and a bottom surface. A plurality of input **bond** pads and output **bond** pads on the upper surface of the semiconductor chip and along the ~~circumference~~ **perimeter** of the semiconductor chip are electrically connected to the semiconductor chip. A chip paddle is provided which has a top surface, a side surface and a bottom surface. The chip paddle is bonded to the bottom surface of the semiconductor chip by an adhesive. The chip paddle has corners, a ~~circumference~~ **perimeter** and a half-etched section at the lower edge of the chip paddle along the chip paddle ~~circumference~~ **perimeter**.

[0009] A leadframe is provided having a plurality of tie bars. Each of the tie bars has a side surface and a bottom surface. ~~The plurality of~~ **Each of the** tie bars ~~are~~ **is** connected to the corners of the chip paddle~~. The plurality of tie bars~~ **and** externally extend**s** from the chip paddle and ~~have~~ **has** a half-etched section. A plurality of dam bars ~~are~~ **is** provided on the leadframe **to** help limit flow of encapsulation material on the leadframe.

[0010] A plurality of internal leads connects to the leadframe. Each of the leads has a side surface and a bottom surface. The leads are radially formed at regular intervals along and spaced apart from the ~~circumference~~ **perimeter** to the chip paddle and extend

towards the chip paddle. Each of the leads has a step shaped half-etched section facing the chip paddle.

[0011] A ground ring is provided having an upper surface and a lower surface, and positioned between the semiconductor chip and the plurality of internal leads. The ground ring may interchangeably be used as a ground or a power ring. The upper surface of the ground ring is substantially planar with the upper surface of the semiconductor chip and the upper surface of the plurality of internal leads. A plurality of ~~via~~ conductive wires ~~are~~ **is** electrically connected to the plurality of internal leads and the semiconductor chip, wherein the conductive wires have a loop height between the leads and the semiconductor chip. Because of the planarity of the grounding leads and ~~semi-conductor~~ **semiconductor** chip, the loop height of the conductive wires is minimized, which allows smaller packaging.

[0012] Encapsulating material encapsulates the semiconductor chip, conductive wires, chip paddle, and the leads to form a package body. The flow of the encapsulation material is limited by the dam bars formed on the leadframe. After encapsulation, the chip paddle, leads, and tie bars are externally exposed at respective side and bottom surfaces. The chip paddle further has through-holes in the half-etched section of the chip paddle for increasing the bonding strength of the encapsulation material in the package body. In addition, tabs in the half-etched section of the chip paddle may be provided for the same purpose.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] A more complete understanding of the method and apparatus of the present invention may be obtained by reference to the following detailed description **with like reference numerals referring to like elements** when taken in conjunction with the accompanying Drawings wherein:

[0014] FIGURE 1 is a top plan view of **one embodiment of** the semiconductor ~~chip~~ **package** of the present invention;

[0015] FIGURE 2 is a side elevation cross-section view of the semiconductor ~~chip~~ **package** of FIGURE 1 taken along line 2-2;

[0016] FIGURE 3 is a side elevation cross-section view of the semiconductor ~~chip~~ **package** of FIGURE 1 taken along line 3-3;

~~**[0017]** FIGURE 4 is a top plan view of a leadframe for one embodiment for the semiconductor package of the present invention;~~

[0018] FIGURE ~~5~~ **4** is a top plan view of an alternate embodiment for the semiconductor package of the present invention; and

[0019] FIGURE ~~6~~ **5** is a side elevation cross-section view of the semiconductor package of FIGURE ~~5~~ **4** taken along line 6-6.

DETAILED DESCRIPTION **OF THE INVENTION**

[0020] Referring first to FIGS. 1 through 3, a semiconductor package 10 is shown construed in accordance with the principals of the present invention. ~~A~~ **The** semiconductor package 10 includes a semiconductor chip 20 having an upper surface 30, a ~~circumference~~ **perimeter** 40 and a bottom surface 50. A plurality of input **bond** pads 60 and output **bond** pads 70 ~~are~~ **is** disposed on the upper surface 30 of the semiconductor chip 20. A chip paddle 80 having a top surface 90, a side surface 100 and a bottom surface 110 is secured to the bottom surface 50 of the semiconductor chip 20 via an adhesive 120. The chip paddle 80 has corners 130, a ~~circumference 140~~ **perimeter 140** ~~(Fig. 4)~~ and a half-etched section 150. The half-etched section 150 is located at a lower edge 160 of the chip paddle 80.

[0021] Referring now to FIGS. 1 through ~~4~~ **3** in combination, a leadframe 170 is shown having a plurality of tie bars 180, a side surface 190 and a bottom surface ~~200.~~ **(not shown)**. The tie bars 180 are connected to the corners 130 of the chip paddle 80. The tie bars 180 externally extend from the chip paddle 80. The leadframe 170 further has a ~~half-etched section 210 and a~~ plurality of dam bars 220.

[0022] A plurality of leads 230 are connected to the leadframe 170 and have an upper surface 235 and a bottom surface 250. The leads 230 are radially formed at regular intervals along the ~~circumference~~ **perimeter** 140 and spaced apart from the ~~circumference~~ **perimeter** 140 of the chip paddle 80. The leads 230 extend towards the chip paddle 80, such that each of the plurality of leads 230 has a half-etched section 260

facing the chip paddle 80. It is to be noted that the hatched areas in FIG. 1 are the half-etched sections of the paddle 80 and leads 230.

[0023] Referring to FIG. 2, there is disclosed a ground ring 262 formed in the half-etched section 150 of the chip paddle 80. The ground ring 262 is positioned between the semiconductor chip 20 and the plurality of leads 230. The ground ring **262** may be interchangeably used as a power ring should circumstances require. The upper surface 264 of the ground ring 262 is planar with the upper surface **90** of the ~~semiconductor chip 20~~ **chip paddle 80** and the upper surface ~~236~~ **235** of the leads 230.

[0024] A plurality of ~~via~~ conductor wires 270 ~~are~~ **is** provided and electrically connected to the plurality of leads 230 and the semiconductor chip 20. The plurality of conductive wires 270 have a loop height 275 between the plurality of leads 230 and the semiconductor chip 20. The loop height 275 of the conductive wires 270 is minimized from the upper surface 235 of the leads 230 and the upper surface 30 of the semiconductor chip 20.

[0025] To form the semiconductor package 10, encapsulation material 280 encapsulates the semiconductor chip 20, conductive wires 270, chip paddle 80, and leads 230. The dam bars 220 limit the flow of the encapsulation material 280 on the leadframe 170. During encapsulation, the chip paddle 80, leads 230, and tie bars 180 are externally exposed at the respective side and bottom surfaces. In ~~a first~~ **one** embodiment, the chip paddle 80 is provided with a plurality of through holes 300 in the half-etched section 150 for increasing the bonding strength of the encapsulation material 280 with the package 10.

[0026] The through holes 300 **(Fig. 1)** may be formed by chemical etching, such as when patterning the entire leadframe 170 for forming the half-etched section 150 of the chip paddle 80. Alternatively, the through holes 300 **(Fig. 1)** may be formed by the use of a mechanical punch or similar device. It should be noted that other methods may be used to form the through holes 300, and the **various embodiments of the** present invention ~~is~~ **are** not limited by the formation techniques disclosed herein.

[0027] Referring now to ~~FIGS. 4 and 5 in combination,~~ **Fig. 4 and FIG. 5,** an alternate embodiment for ~~the~~ **a** semiconductor package ~~10~~ **11** is shown. In this embodiment, the chip paddle 80 is provided with a plurality of tabs 310 in the half-etched

section 150 of the chip paddle 80 for the similar purpose of increased bonding strength. It is also contemplated that the combination of through holes 300 **(Fig. 1)** and tabs 310 may be used to increase the bonding strength of the encapsulation material 280 in the package 10.

[0028] The tabs 310 are formed in the half-etched section 150 of the chip paddle 80. The tabs 310 must extend~~ed~~ to a limited degree to prevent a short circuit forming between the tabs 310 and the leads 230. It is preferable that the number of the tabs 310 corresponds to the number of the grounding input **bond** pads 60 and output **bond** pads 70 of the semiconductor chip 20. The tabs 310 may be formed by chemical etching when patterning the entire leadframe ~~170~~ **171** and also by other mechanical methods depending on the requirements of the individual package ~~10.~~**11.** By increasing the area or length of the chip paddle 80, the tabs 310 are easily bonded with conductive wires 270 by increasing the area for which to connect the conductive wires 270. The tabs 310 may serve to function as a ground or power ring ~~262~~ in certain applications. It is to be noted that the hatched areas in FIG. ~~5~~ **4** are the half-etched sections of the paddle 80 and leads 230.

[0029] **The tab 310 is electrically connected to the semiconductor chip 20 via conductive wire 270.**

[0030] As described previously, the use of the through holes 300 and tabs 310 increase**s** the bonding strength to the encapsulation material 280, in addition to improving the fluidity of the encapsulation material 280 upon encapsulating. The presence of the through holes 300 and tabs 310 improves the fluidity of encapsulation material 280 by directing flow over or through the tabs 310 and through holes 300 in the package 10. In certain embodiments, as shown in FIGS. 2 and 3, a plated layer 320 may be applied to the upper surfaces 90, 235 of the chip paddle 80 and leads 230, respectively, to increase bonding strength to the wires 270.

[0031] It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. While the semiconductor package having improved adhesiveness and crown bonding shown as described ~~as being~~ **is** preferred, it will be obvious to a person of ordinary skill

in the art ~~to add~~ **that** various changes and modifications may be made therein without departing from the spirt and scope of the invention.

[0032] The previous description is of a preferred embodiment for implementing the invention, and the scope of the invention should not necessarily be limited by this description. The scope of the present invention is instead defined by the following claims.

[0033] The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein:

~~Attorney Docket~~ U.S. Patent No.	Title of Application	First Named Inventor
~~45475-00015~~ 6,501,161	Semiconductor Package Having Increased Solder Joint Strength	Kil Chin Lee
~~45475-00016~~ 6,667,662	Clamp and Heat Block Assembly for Wire Bonding a Semiconductor Package Assembly	Young Suk Chung
~~45475-00018~~	~~Semiconductor Package~~	~~Sean Timothy Crowley~~
6,639,308	Near Chip Size Semiconductor Package	Sean Timothy Crowley
~~45475-00019~~ 6,753,597	Semiconductor Package	Sean Timothy Crowley

~~45475-00020~~ **6,605,866**	Stackable Semiconductor Package and Method for Manufacturing Same	Sean Timothy Crowley
~~45475-00021~~ **6,730,544**	Stackable Semiconductor Package and Method for Manufacturing Same	Jun Young Yang
~~45475-00024~~ **6,616,436**	Method of and Apparatus for Manufacturing Semiconductor Packages	Hyung Ju Lee
~~45475-00029~~ **6,555,899**	Semiconductor Package Leadframe Assembly and Method of Manufacture	Young Suk Chung

[0034] It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred exemplary embodiments. It will be obvious to a person of ordinary skill in the art that various changes and modifications may be made herein without departing from the spirit and scope of the invention.